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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/063,295	04/09/2002	Wagdi William Abadeer	BUR920010127	4885

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EXAMINER	
SHINGLETON, MICHAEL B	
ART UNIT	PAPER NUMBER
2817	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10-063,295	Abadeer et al.
	Examiner	Group Art Unit
	SHINGLETON	2817

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE Three MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

☐ Responsive to communication(s) filed on _____.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1-20 is/are pending in the application.

Of the above claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-20 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement

Application Papers

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☒ The drawing(s) filed on 6-12-2002 is/are ~~objected to~~ acceptable by the Examiner

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119 (a)-(d).

☐ All ☐ Some* ☐ None of the:

☐ Certified copies of the priority documents have been received.

☐ Certified copies of the priority documents have been received in Application No. _____.

☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a))

*Certified copies not received: _____.

Attachment(s)

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 4

☒ Notice of Reference(s) Cited, PTO-892

☐ Notice of Draftsperson's Patent Drawing R view, PTO-948

☐ Interview Summary, PTO-413

☐ Notice of Informal Patent Application, PTO-152

☐ Other _____

Office Action Summary

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4 and 7 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Buer et al. 6,272,439 (Buer).

Figure 4 of Buer discloses a ring oscillator (See column 7, around line 16) having an odd number of elements. Note that Buer states that any number of elements can be selected (See column 7, around line 21). Figure 4 clearly shows these odd number of elements interconnected in a serially-connected infinite loop with each of the elements 104-110 having an associated programmable delay. The enable signal 312 is applied at the input of the gate 412 for turning on and off oscillation and thus this input "starts an oscillation". The input to the encoder 406 forms an input to receive an input signal to program (adjust) each of the programmable delays. Buer states that the delay cells, i.e. "elements" in claim terminology, can be implemented using any number of different elements including non-inverting buffers which are non-inverting amplifiers. Thus each of these elements comprises a non-inverting amplifier as claimed. (See column 7 around line 37). The register inherently produces a binary word as this is what a register does and this binary word serves as a "vector input" which determines the programmable delay.

Claims 9-12, 14 and 16 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by La Rosa et al. 6,476,632 (La Rosa).

La Rosa discloses a test circuit that measures device degradation mechanisms such as Negative Bias Temperature Instability effect (NBTI) by its correlation to measured RO (Ring Oscillator) degradations (Note the entire document.) This measured effect is for both NMOSFETs and PMOSFETs (Note the use of CMOS technology in the making of the RO. Column 4, around line 38.). Various stressing such as DC, AC and "free-running mode" stressing are used to determine this correlation and in particular the AC stressing includes having the gate of the target PFET receive the varying voltage (Note columns 7-11). A target PFET in element IS-Y is choose to apply these tests or stress to. La Rosa

throughout its entire disclosure describes on chip performance and thus the RO is inherently integrated in order for this to occur. The RO has an odd number of oscillator elements (See column 7 around line 45 for example.). Figure 9 clearly shows the odd number of oscillator elements interconnected serially in an infinite loop. Numerous test outputs are provided as describe at least in part by Table 1, for example node V2 is used to measure current which is "at least one parameter" of the RO. All the oscillator elements are CMOS and thus each one contains a "target PFET". The pass gates of La Rosa are switches that are part of a switching circuit and are selectively switched with respect to at least one stress condition (Note columns 7-11). The claimed method steps of testing are clearly present in the structure as noted above. For example, as noted above, the target PFET is provided in a RO that consists of an odd number of elements. Also as noted above at least one stress test is preformed on the PFET and at least one characteristic of the RO is measured. As noted above the test is for the NBTI effect on the target PFET.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Buer et al. 6,272,439 (Buer) in view of Rothermel 5,448,205 (Rothermel).

All the same reasoning as applied to claims 1-4 and 7 and the following: Buer is silent on the use of programmable delays for each of the "elements" that varies the delay in such a manner so as to adjust the duty factor of the output signal of the ring oscillator.

Figure 1 of Rothermel shows one example of a ring oscillator that controls the delay elements i.e. the amplifiers/inverters of Rothermel. Rothermel also teaches that the delay time of each of these elements can be individually adjusted so as to vary the oscillatory period and/or the duty factor (See column 8 around line 18).

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide each element with a variable delay time and control this time so as to allow for the adjustment of the duty factor of the ring oscillator as taught by Rothermel.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Buer et al. 6,272,439 (Buer).

All the same reasoning as applied to claims 1-4 and 7 and the following: Buer is silent on the construction of the non-inverting amplifier/buffer elements as being formed from CMOS technology. As noted above any type of delay element can be employed as specifically mentioned by Buer (See column 7, around line 35). One common art recognized equivalent non-inverting amplifier/buffer are those formed from CMOS technology. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have employed non-inverting CMOS amplifiers/buffers for the elements of Buer because, as the Buer reference is silent on the specifics of the non-inverting amplifier/buffer structure, any art recognized equivalent non-inverting amplifier/buffer would have been usable therewith such as the conventional non-inverting CMOS amplifier/buffer structure.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over La Rosa et al. 6,476,632 (La Rosa).

All the same reasoning as applied to claims 9-12, 14 and 16 and the following: LaRosa is silent on the exact form of the varying signal applied to the gate of the target PFET. The use of a pulse to AC stress an element wherein that pulse is adjustable in at least one of frequency and duty factor is a conventional and well-known.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used a pulse wherein the pulse is adjustable in at least one of frequency and duty factor in place of the varying signal applied at the gate of the target PFET in LaRosa because, as the LaRosa reference is silent on the exact shape of the waveform employed, any art recognized equivalent varying signal would have been useable therewith such as the conventional pulse waveform that is adjustable in at least one of frequency and duty cycle.

Claims 8, 15, and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over La Rosa 6,476,632 (La Rosa) in view of Buer et al. 6,272,439 (Buer).

La Rosa discloses a test circuit that measures device degradation mechanisms such as Negative Bias Temperature Instability effect (NBTI) by its correlation to measured RO (Ring Oscillator) degradations (Note the entire document.) This measured effect is for both NMOSFETs and PMOSFETs (Note the use of CMOS technology in the making of the RO. Column 4, around line 38.). Various stressing such as DC, AC and "free-running mode" stressing are used to determine this correlation and in particular the AC stressing includes having the gate of the target PFET receive the varying voltage (Note columns 7-11). A target PFET in element IS-Y is choose to apply these tests or stress to. La Rosa

throughout its entire disclosure describes on chip performance and thus the RO is inherently integrated in order for this to occur. The RO has an odd number of oscillator elements (See column 7 around line 45 for example.). Figure 9 clearly shows the odd number of oscillator elements interconnected serially in an infinite loop. Numerous test outputs are provided as describe at least in part by Table 1, for example node V2 is used to measure current which is "at least one parameter" of the RO. All the oscillator elements are CMOS and thus each one contains a "target PFET". The pass gates of La Rosa are switches that are part of a switching circuit and are selectively switched with respect to at least one stress condition (Note columns 7-11). The claimed method steps of testing are clearly present in the structure as noted above. For example, as noted above, the target PFET is provided in a RO that consists of an odd number of elements. Also as noted above at least one stress test is preformed on the PFET and at least one characteristic of the RO is measured. As noted above the test is for the NBTI effect on the target PFET. La Rosa is silent on the providing of a programmable delay to the "elements" of the RO. The above structure also clearly provides the claimed method steps of claim 15 which includes incorporating a target PFET into a ring oscillator having an odd number of elements, performing at least one stress test on the PFET and measuring the at least one characteristic of the ring oscillator. LaRosa as indicated above is silent on the "step" having a variable delay for the elements of the RO.

Buer teaches that it is well known to provide programmable delays for each of the delay cells what applicant refers to as "elements" in the claims. This makes the RO adjustable, mostly in frequency (See the entire specification of Buer especially column 4, around line 5).

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide programmable delays to each of the "elements" in La Rosa so as to make the RO adjustable and allow for changing of the frequency as taught by Buer.

LaRosa is silent on using the test results to adjust a design of [a] MOSFET device(s) by using the measurements to predict, and "modify a design parameter of said target PFET" so as to improve reliability(Decrease degradation over time.) or correct a manufacturing process. It is common-knowledge in the art that one reason for testing a device is so that one determines the limits of that device so that designers can determine what to modify so as to improve device parameters. In other words in order to improve device parameters one must first measure the device parameters.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the test results to "modify a design parameter of said target PFET" so as to improve reliability or correct a manufacturing process to improve reliability since it was known in the art that test results are used to aid designers in designing of improved devices.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hur et al. and Srivastava et al. both disclose various forms of ring oscillators.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is 703-308-4903. The examiner can normally be reached on Monday-Thursday from 8:00 to 4:30. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (703) 308-4909. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

MBS
July 8, 2003

MICHAEL B SHINGLETON
PRIMARY EXAMINER
GROUP ART UNIT 2817